

APPLICATION FOR UNITED STATES LETTERS PATENT

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TITLE: STACKED SEMICONDUCTOR PACKAGE AND FABRICATING
METHOD THEREOF

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STACKED SEMICONDUCTOR PACKAGE AND FABRICATING METHOD
THEREOF

BACKGROUND OF THE INVENTION

5 1. Field of the Invention

The present invention relates to a stacked semiconductor package, and a fabricating method thereof.

10 2. Background of the Related Art

Figures 1A through 1D illustrate an example of a background art method of forming stacked semiconductor packages. Figure 1A shows a cross-sectional view of an upper thin small outline (TSO) package 1 and a lower TSO package 2, each TSO package being fabricated by packaging two semiconductor chips with a molding resin. Outer leads 3 are formed on outer ends of each TSO package 1, 2. Those TSO packages 1, 2 can be distinguished by the shape of their outer leads 3. As a result of a stacking process, a plurality of leads 3 are formed on opposite sides of the upper and lower TSO packages 1, 2.

15 Figure 1B shows the upper TSO package 1 stacked to an upper side of the lower TSO package 2. A nipper 4 picks up the stacked TSO packages 1, 2, as shown in Figure 1C, and the leads 3 are dipped in a solder solution 5 in a vessel 6 such that a connecting portion of the outer leads 3 of the stacked TSO packages 1, 2 is covered with the solder solution 5. The solder solution 5 is heated to its boiling point at approximately 250°C. To prevent the plurality of outer leads 3 from inadvertently contacting one another, each outer lead is soldered separately.

During the soldering process, the outer leads 3 of the TSO packages 1, 2 are dipped in the solder solution 5 or smeared with drops splashed from the boiling solder solution 5. The stacked TSO package is completed once the solder solution at the outer leads 3 of the upper and lower TSO packages 1, 2 is made to reflow, as illustrated in Figure 1D.

5 The background art method has various disadvantages. It is difficult to control the amount of solder solution which contacts the stacked TSO package, because the outer leads are dipped in the solder solution or smeared with the drops splashed from the boiling solder solution. In addition, when a plurality of the outer leads are densely packed together, it is more difficult to separately dip each outer lead in the solder solution, and short-circuiting can 10 result when adjacent outer leads are connected to one another by the solder solution.

SUMMARY OF THE INVENTION

It is an object of the present invention to provide a method of forming a stacked semiconductor package, similar in size to a semiconductor chip, which is easier to perform than 15 background art methods.

It is also an object of the present invention to provide a method of forming a stacked semiconductor package which can prevent short-circuiting that can occur when terminals are inadvertently connected to one another.

A stacked semiconductor package embodying the present invention includes first and 20 second semiconductor chips having first sides, wherein a plurality of chip pads are formed on the first sides of the chips, and a bonding tape is adhered to the first and second chips, the

bonding tape having conductive interconnections that couple corresponding chip pads of the first and second semiconductor chips. A package embodying the invention may also include a plurality of conductive media which are used to couple the chip pads to external devices. A package embodying the invention may be configured such that the first sides of the chips are 5 substantially parallel to one another with the first sides being arranged on either the external sides of the package, or so that they face one another inside the package. A heat conducting plate may also be connected between the first and second chips.

A device embodying the invention may also comprise a bonding tape for joining two semiconductor chips. The bonding tape would include a flexible adhesive layer configured 10 so that it can be adhered to first surfaces of first and second semiconductor chips to attach the chips to each other. The bonding tape would also include a plurality of conductive regions formed on the adhesive layer such that when the adhesive layer is adhered to the first and second semiconductor chips, the conductive regions will electrically couple chip pads on the first semiconductor chip to corresponding chip pads on the second semiconductor chip.

15 A method embodying the invention includes the steps of attaching a first semiconductor chip to a second semiconductor chip using a bonding tape that adheres to first surfaces of the chips, wherein conductive interconnections on the bonding tape also electrically couple corresponding chip pads formed on the chips. The method also includes bending the bonding tape such that the first surfaces of the first and second semiconductor chips are arranged 20 substantially parallel to one another. A method of bonding the invention can also include a step of attaching a plurality of conductive media to the conductive interconnections on the

bonding tape such that the plurality of conductive media can serve as external leads of the package.

An alternative method of forming a stacked semiconductor package, embodying the invention, includes a first step of sawing a wafer on which a plurality of semiconductor chips are arranged in pairs to separate the wafer into a plurality of chips; adhering a bonding tape to the chips so that the bonding tape attaches adjacent pairs of chips to one another, and so that conductive interconnections on the bonding tape electrically connect respective chip pads of adjacent pairs of the chips; cutting the bonding tape; and stacking the pairs of semiconductor chips so that they face each other. Some methods embodying the invention may include an additional step of adhering conductive media to the bonding tape. Also, the wafer may be attached to an adhesive mounting foil before the wafer is cut into individual chips.

Additional advantages, objects, and features of the invention will be set forth in part in the description which follows and in part will become apparent to those having ordinary skill in the art upon examination of the following or may be learned from practice of the invention.

The objects and advantages of the invention may be realized and attained as particularly pointed out in the appended claims.

BRIEF DESCRIPTION OF THE DRAWINGS

The invention will be described in detail with reference to the following drawings in which like reference numerals refer to like elements, and wherein:

Figures 1A through 1D illustrate a background art fabricating process for a stacked TSO package;

Figures 2A through 2D illustrate a fabricating process for a stacked semiconductor package according to the present invention, where Figure 2A shows a perspective view of two semiconductor chips prior to stacking, Figures 2B and 2C show plan views of a wafer, and Figure 2D shows a plan view of the two semiconductor chips prior to stacking;

Figure 3A illustrates a perspective view of a stacked semiconductor package according to a first embodiment of the present invention;

Figure 3B illustrates a perspective view of a stacked semiconductor package according to a second embodiment of the present invention; and

Figure 3C illustrates a perspective view of a stacked semiconductor package according to a third embodiment of the present invention.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

Figures 2A through 2D illustrate a fabricating process of a stacked semiconductor package according a preferred embodiment of the present invention. Figure 2A shows a perspective view of two semiconductor chips 10 prior to stacking. A plurality of chip pads 21 are formed on first sides 11 of the pair of semiconductor chips 10. Additionally, the semiconductor chips 10 are configured to have a second side 12 opposite to the first side 11, a near side edge 13 adjacent to the chip pads 21, and a far side edge 14 opposite the chip pads 21. The near and far side edges 13, 14 run parallel to a forming direction of the chip pads 21,

while top and bottom side edges 15 run perpendicular to the forming direction of the chip pads 21.

Figure 2B shows a plurality of semiconductor chips 10 configured on a first side of a wafer 20. The chips are formed such that the chip pads 21 of adjacent pairs of chips 10 are 5 adjacent to each other. The wafer 20 is positioned on an adhesive mounting foil (not shown).

To form a package embodying the invention, the wafer 20 must be cut at a thickness equal to a desired distance 22 between the semiconductor chips 10. The wafer 20 on the mounting foil is cut along the boundaries of the respective semiconductor chips 10. The adjacent pairs of chips can be stacked together in different ways, and the stacking method 10 dictates the thickness 22 of the cut between adjacent chips. The distance 22 between a pair of semiconductor chips 10 may equal a distance 23, or a distance 24, as shown in Figure 3A and Figure 3B. After cutting, the adhesive mounting foil prevents the semiconductor chips 10 from moving relative to one another, and thus maintains the shape of the wafer 20. As a result, it is easier to adhere a bonding tape to pairs of the semiconductor chips 10, as discussed 15 in more detail below.

Figure 2C illustrates a tape-automated bonding (TAB) process. A bonding tape 26 is adhered between pairs of semiconductor chips 10. The bonding tape 26 is attached to the first sides of the chips 20 such that conductive interconnections 25 formed on one side of the bonding tape 26 connect corresponding chip pads 21 of adjacent pairs of chips 10. Next, 20 the bonding tape 26 is cut along cutting lines 27, and each pair of semiconductor chips 10 is separated from the mounting foil.

Figure 2D shows an enlarged plan view of a pair of semiconductor chips 10 after separation from the mounting foil, and before stacking has been completed. Corresponding chip pads 21 of the two chips 10 are electrically connected by the conductive interconnections 25, formed on the bonding tape 26. Predetermined regions 40 of the conductive interconnections 25 may be silver-plated. Solder balls 31 or other conductive media can then be mounted at those plated regions 40.

In the embodiment shown in Figure 2D, the plated regions 40 are configured in an alternating pattern so that one solder ball can be attached to each conductive interconnection 25, and so that the solder balls are spread apart when the package is completed. The silver plating electrically connects the adhesive and non-adhesive sides of the bonding tape 26. Accordingly, when the conductive interconnections 25 formed on the adhesive side of the bonding tape 26 are connected with the respective chip pads 21 formed on the semiconductor chips 10, the chip pads 21 can transmit electrical signals to solder balls attached to the plated regions 40 via the conductive interconnections 25. The solder balls function as outer terminals. Of course, other types of conductive media could be used in place of the solder balls.

An attached pair of semiconductor chips 10 is stacked by bending the bonding tape 26 twice in a perpendicular manner such that the first sides 11 of the chips 10 run parallel to each other. The arrangement of stacked semiconductor package may be varied by bending the bonding tape 26 in different directions.

Figure 3A shows a first embodiment of the present invention where the first sides 11, and thus the chip pads 21, are externally positioned. After the bonding tape 26 is bent such that the first sides 11 of the pair of semiconductor chips 10 are externally exposed, a plate 28 is adhered between the pair of semiconductor chips 10 using a non-conductive two-sided adhesive tape 29, thereby stacking the semiconductor chips 10.

As described above, when the first sides 11 are externally positioned after the bonding tape 26 has been bent perpendicularly twice, the near side edges 13 of the semiconductor chips 10 are in contact with the bonding tape 26. The plate 28 is adhered using the non-conductive two-sided adhesive tape 29 on the second sides 12 of the semiconductor chips 10.

The plate 28 attached to the second sides 12 of the semiconductor chips 10 may leave a predetermined space between an end of the plate 28 and the conductive interconnections 25 of the bonding tape 26. A liquid-phase epoxy molding compound 30 is injected into that predetermined space. The bonding tape 26 thus adheres to the near side edges 13 of the semiconductor chips 10 and the epoxy molding compound 30, in addition to the chip pads 21 and first sides 11. Solder balls 31, or other types of conductive media, are then positioned on the outer surface of the bonding tape 26.

Figure 3B shows a second preferred embodiment of the present invention where the first sides 11 and the chip pads 21 of the pair of semiconductor chips 10 are internally positioned. After the bonding tape 26 is bent such that the second sides 12 are externally exposed, the plate 28 is adhered between the pair of semiconductor chips using a non-conductive two-sided adhesive tape 29, thereby stacking the semiconductor chips 10.

The plate 28 attached to the first sides 11 of the semiconductor chips 10 leaves a predetermined space between the plate 28 and the conductive interconnections 25 of the bonding tape 26. A liquid-phase epoxy molding compound 30 is injected into the predetermined space. Solder balls 31 are then attached to the exposed surface of the bonding tape 26.

5 In the first and second preferred embodiments of the present invention, the plate 28 helps to discharge heat generated from operation of the semiconductor chips 10. The plate 28 may be made of metal, or any other material that readily conducts heat. The plate may be between about 0.1mm and about 0.3mm thick, which is approximately the thickness of the semiconductor chips 10. A portion of the plate 28 is externally exposed when the pair of semiconductor chips 10 are stacked. The length of the exposed portion is determined based on the heat discharge efficiency and the size of the stacked semiconductor package. Thus, a larger exposed portion of the plate 28 from the stacked semiconductor chips 10 corresponds to a higher efficiency of heat discharge. However, the size of the stacked semiconductor package increases.

15 In addition, the distance 22 between pairs of semiconductor chips formed on a wafer (see Figure 2B) equals a distance 23, 24 between the first sides 11 of the semiconductor chips 10 after the package has been formed. Thus, that distance 22 is different in the first and second preferred embodiments of the present invention.

20 The semiconductor chip 10 thickness is represented by 'δ' and the thickness of the metal plate 28 and the non-conductive two-side adhesive tape 29 is represented by 'D.' In the first preferred embodiment of the present invention, the distance 22 between a pair of

semiconductor chips 10 on the wafer 20 equals the distance $(D+2\delta)$ 23 between the first sides 11 of the semiconductor chips 10 in the fabricated stacked semiconductor package, as shown in Figure 3A. However, in the second preferred embodiment of the present invention, the distance 22 between a pair of semiconductor chips 10 on the wafer 20 equals the distance (D) 5 24 between the first sides 11 of the pair of semiconductor chips 10 in the fabricated stacked semiconductor package, as shown in Figure 3B. Therefore, the distance 24 according to the second preferred embodiment is less than the distance 23 according to the first embodiment.

Figure 3C shows a third preferred embodiment of the present invention. In this embodiment, the pair of semiconductor chips 10 are stacked without using a plate, and the non-conductive two-sided adhesive tape 29 holds the chips 10 together, and prevents the chips 10 from contacting one another. Thus, the stacked semiconductor package can be made smaller and thinner due to the reduced distance D between the adjacent semiconductor chips 10. Additionally, the bonding tape 26 does not require separation from a plate, and thus, the step of injecting an epoxy molding compound between the plate and bonding tape is eliminated. 15 However, the heat discharge efficiency is decreased. The solder balls 31, which serve as outer terminals, are then mounted on the silver-plated predetermined regions 40 of the bonding tape 26, thus completing the stacked semiconductor package fabrication process.

An additional embodiment of the invention, similar to the one shown in Figure 3C, could also be made by stacking two semiconductor chips 10 such that their first sides 11 are 20 located internally and face one another. This embodiment would have its chips 10 arranged

as shown in Figure 3B, except the chips would be directly attached to one another with a double sided adhesive. This embodiment would not have the plate 28 shown in Figure 3E.

A stacked semiconductor package embodying the present invention has various advantages. Attaching the semiconductor chips using one-sided adhesive bonding tape with the conductive interconnections simplifies the process of attaching the chips to each other, and of coupling corresponding chip pads. Thus, the present invention obviates the disadvantages of the background art caused by stacking and electrically connecting the semiconductor chips by dipping the outer leads in a solder solution, including short-circuiting of the leads.

In addition, a chip size package can be formed using a plate similar in thickness to the semiconductor chip, or by stacking the semiconductor chips without the plate. Use of the plate helps to discharge heat generated by the semiconductor chips, thus improving heat discharge efficiency.

The foregoing embodiments are merely exemplary and are not to be construed as limiting the present invention. The present teaching can be readily applied to other types of apparatuses. The description of the present invention is intended to be illustrative, and not to limit the scope of the claims. Many alternatives, modifications, and variations will be apparent to those skilled in the art. In the claims, means-plus-function clauses are intended to cover the structures described herein as performing the recited function and not only structural equivalents but also equivalent structures. For example, although solder balls and metal leads may not be structural equivalents in that a solder ball has a lower melting point and smaller

external dimensions than a metal lead, in the environment of providing electrical connections to a chip package, a solder ball and a metal lead may be equivalent structures.